

FEATURES

- DC, gain, time skew and bandwidth background calibration
- Digital, analog and hybrid time skew correction modes
- Wideband operation
 - 90% of Nyquist band
 - Multiple Nyquist zones

- 10-bit to 18-bit ADC resolution
- Low power and high-speed

APPLICATIONS

- Wideband communication receivers
- High-end test and measurement digitizers

DESCRIPTION

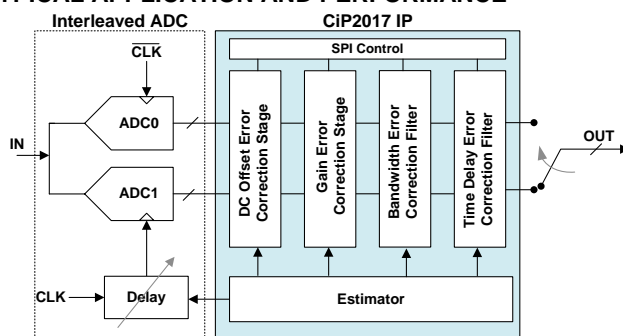
CiP2017 is a proven digital IP for background calibration of mismatch errors in 2-channel, time-interleaved A/D converters. It provides wideband interleaving spurs rejection while maintaining low power and high-speed thanks to Cerasic Zero-Spurs technology. It has many features that can be enabled through SPI interface and that allow the IP to address most applications. Additional custom features can be added upon request.

DC, gain, time skew and bandwidth errors are estimated continuously in the digital domain to track drifts with temperature for instance. They feed a correction engine that supports digital, analog and hybrid operating modes. In digital correction mode, time skew compensation is performed with a low latency digital FIR filter. In analog correction mode, the digital correction filter is disabled and the estimator is still active. The estimated time skew error is used to control a digitally tunable time delay in the clock path and form a closed estimation-correction loop.

Hybrid time skew correction mode uses a digital filter for fine time skew tuning in combination with a low complexity analog delay for coarse time skew adjustment. This digital-analog approach provides high dynamic range and large correction range while preserving jitter performance of the clock path at high frequencies. The resolution split between analog and digital is programmable through SPI interface.

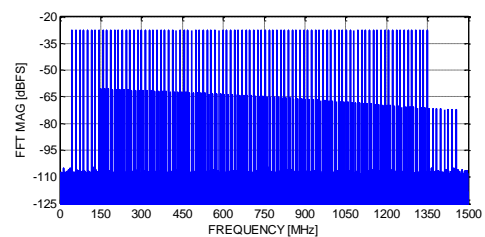
CiP2017 IP integrates a digital filtering stage for bandwidth error correction. The coefficients of the digital filter are estimated online. This feature is suitable for applications where bandwidth spurs cannot be ignored and may drift over time. This situation occurs for instance in on-board time-interleaved ADCs at high operating frequencies.

TYPICAL APPLICATION AND PERFORMANCE

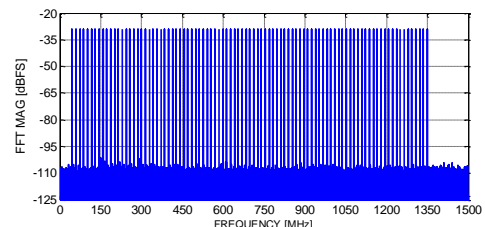


Test case: a wideband, multi-tone signal is used to test a simulated 14-bit/3Gsps/64dB SNR/3GHz BW, time-interleaved ADC with 0.1dB, 3.5ps and 110MHz gain, time skew and bandwidth errors respectively. Interleaving spurs limited the SFDR to -60dBFS before calibration. CiP2016 IP cancelled effectively these spurs and improved SFDR to -100dBFS.

Before Calibration



After Calibration



As a digital IP, CiP2017 can be fully characterized with simulation data that has the benefit of reproducing any use case that is beyond the capability of commercially available A/D converters. However, Cerasic IPs have been validated also with measured data from actual ADCs. Cerasic R&D team has system design and test expertise to design a custom demonstrator upon request.

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